ABSTRACT OF THE DISCLOSURE

A memory cell transistor using a word line **WL** as the gate thereof is provided in an active region **OD**, and a ferroelectric capacitor, including bottom electrode, ferroelectric film and top electrode **TE**, is formed on a field oxide film. A first interconnection layer is made up of storage lines, each connecting the top electrode **TE** to one of doped layers of the memory cell transistor, and bit lines, each of which is connected to the other doped layer. In a planar layout, the storage line intersects only one side of the top electrode **TE** and the bit line **BL** does not overlap with the top electrode **TE**. Thus, it is possible to prevent the retention characteristics of the ferroelectric capacitor from being deteriorated due to the stress applied by the first interconnection layer to the ferroelectric capacitor. As a result, the reliability of a ferroelectric memory device, including, in a memory cell, a ferroelectric capacitor with a ferroelectric film interposed between the bottom and top electrodes, can be improved.